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Derwent Title: **Fair packet scheduler through weighted fair queuing(wfq) emulation in high-speed integrated service network and method thereof**

Original Title: ☒ **KR1000087A: FAIR PACKET SCHEDULER THROUGH WEIGHTED FAIR QUEUEING(WFQ) EMULATION IN HIGH-SPEED INTEGRATED SERVICE NETWORK AND METHOD THEREOF**

Assignee: **INFORMATION & COMMUNICATIONS FOUND Non-standard company
UNIV INFORMATION & COMMUNICATIONS Non-standard company**

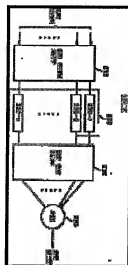
Inventor: **KO N S; KOH N S; PARK H S;**

Accession/Update: **2001-429981 / 200340**

IPC Code: **H04L 12/56 ;**

Derwent Classes: **W01;**

Manual Codes: **W01-A03B(Packet transmission) , W01-A06G2(Stored and forward switching)**



Derwent Abstract: (**KR1000087A**) **Novelty** - A fair packet scheduler through weighted fair queuing (WFQ) emulation in a high-speed integrated service network and method thereof, is provided to maintain a counting complexity of a system virtual time with zero/one while securing a delay bound and a fair index in a WFQ standard. The fair packet scheduler provides a fair and optimum delay bound, when deciding packet transmission orders based on a traffic contract with a network by connection of each packet entering an asynchronous transfer mode(ATM) exchange or a router.

Detailed Description - An input traffic processor(210) utilizes a system virtual time maintained and managed in a node whenever a new packet arrives at the node to calculate a time stamp, and adds the time stamp to a header of arrived packets. Queue blocks(220-1/220-n) temporarily store the packets processed in the input traffic processor(210) and make the stored packets waited. A start packet processor (230) selects a packet having a smaller time stamp value among the standby head packets. A server(250) transmits the packet selected in the start packet processor (230) according to arrival orders to a link. And the start packet processor(230) updates the system virtual time before a start time of a new service, after the service for the packets in the server(250) is ended.

Images:

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Priority info (Country/Number/Date)	-
Title of invention	고속 통합 서비스망에서 W F Q의 에뮬레이션을 통한 공정패킷 스케줄링 방법 및 그 공정 패킷 스케줄러 (EMULATED WEIGHTED FAIR QUEUEING ALGORITHM FORHIGH-SPEED INTEGRATED SERVICE NETWORKS AND THE SCHEDULER THEREFOR)
Abstract	본 발명은 ATM 또는 인터넷 등의 고속 패킷 교환망에서의 ATM 교환기 또는 라우터 등과 같은 패킷 노드에서 제한된 노드의 처리용량을 복수의 사용요청에 대하여 공정하게 분배하기 위한 공정 패킷 스케줄링(fair packet scheduling) 방법 및 그 스케줄러에 관한 것이다. 본 발명은 노드로 새로이 도착한 패킷에 대한 새로운 서비스의 개시시점 이전에 갱신된 시스템 가상 시간을 시스템 가상시간을 이용하여 타임스탬프를 계산하여 상기 도착 패킷의 헤더에 부가하여 큐에 일시 대기시키는 입력 트래픽 처리부와, 상기 큐에 대기중인 패킷을 갖는 연결의 선두 패킷중 가장 적은 타임스탬프값을 갖는 패킷을 선택하는 출발 패킷 처리부와, 상기 출발 패킷 처리에서 선택된 패킷을 연결별 도착한 순서대로 목적지 망으로 전송하는 서비스층을 수행하는 서버를 포함한다.